REMARKS

The claims are claims 1, 4, 7 and 9.

The application has been further amended to include correction of those errors noted by the Examiner.

Claims 1, 4, 7 and 9 are amended. Claims 2, 3, 5, 6, 8, 10 and 11 are canceled. Claims 1 and 7 are amended to explicitly recite assembly of execute packets that span two fetch packets. Claims 4 and 9 have been amended to closely correspond to the embodiment illustrated in Figure 9 of the application. Claims 1, 4 and 9 have been further amended to respond to the objections of the Examiner.

Claims 1 and 7 were rejected under 35 U.S.C. 102(b) as anticipated by Simar et al European Patent Application EP 0855648A2.

Claims 1 and 7 recite subject matter not anticipated by Simar et al. Claim 1 recites selecting an execute packet "from two fetch packets" "by scanning instructions from lower memory address locations to higher memory address locations beginning in a first fetch packet...continuing past an end of said first fetch packet to a beginning of a second fetch packet until said p-bit of an instruction has said second digital state." Claim 7 similarly recites determining an execute packet by "scanning the p-bit of each instruction of each fetch packet from lowest memory address location in a first memory fetch packet to highest memory address location in a second immediately following fetch packet." Simar et al includes directly contrary language. Simar et al states at page 6, lines 4 and 5:

> "An execute packet cannot cross an 8-word boundary. Therefore, the last p-bit in a fetch packet is always set to 0, and each fetch packet starts a new execute packet."

The Applicants respectfully submit in view of this directly contrary language, that Simar et al fails to anticipate the recitation of scanning from a first fetch packet to a second fetch packet. Accordingly, claims 1 and 7 are allowable over Simar et al.

Claims 4 and 9 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Simar et al and Heishi et al U.S. patent No. 6,324,639.

Claims 4 and 9 recite subject matter not made obvious by the combination of Simar et al and Heishi et al. Claim 4 recites each multiplexer has "a first input receiving an entire instruction from a predetermined section of said first latch, a second input receiving an entire instruction from a corresponding section of said second latch" and selects at its output "said entire instruction from said section of said first latch, said entire instruction from said section of said second latch, or no instruction." Claim 9 recites "selecting an entire instruction from a predetermined section of said first latch, an entire instruction from a corresponding section of said second latch, or no instruction." Heishi et al fails to teach that his multiplexers 224a, 224b, 224c and 224d select instructions only from a predetermined section of the first latch and a corresponding section of the second latch. Figure 8 of Heishi et al clearly shows that each multiplexer 224a, 224b, 224c and 224d is connected at all sections A0, A1, A2 and A3 of instruction buffer A 221 and all sections B0, B1, B2 and B3 of instruction buffer B 222. As a consequence each multiplexer 224a, 224b, 224c and 224d of Figure 8 of Heishi et al requires six inputs, one input from each section A0, A1, A2, A3, B0, B1, B2 and B3 of both instructions buffers 221 and 222. In contrast, the multiplexers recited in claims 4 and 9 require only two inputs, one from a single section of latch stage 910 and one from a corresponding section of latch stage 911. Thus

this invention accomplishes a similar purpose with much simpler hardware. Accordingly, claims 4 and 9 are not made obvious by the combination of Simar et al and Heishi et al.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment is in response to two new rejections, including one rejection based on a reference not previously cited. Thus the Applicant has had no previous opportunity to response to the current rejections

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,

Robert D. Marshall

Robert D. Marshall, Jr.
Reg. No. 28,527